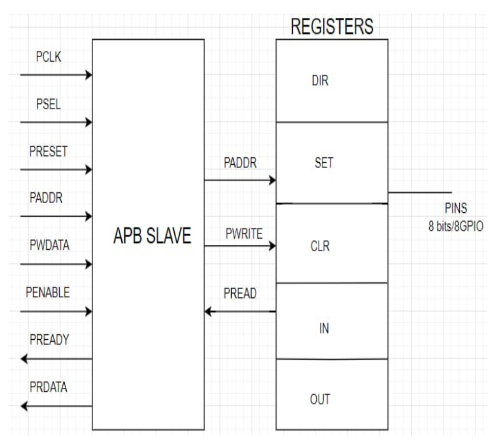
**APB Slave to GPIO: Data sheet**

Functional block diagram

The functional block diagram of APB Slave to GPIO is as shown in the figure 1.

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**Figure 1: Functional block diagram of APB Slave to GPIO**

The functional block diagram illustrating the basic outline of the APB to GPIO is shown in the figure 1. General Purpose Inputs Outputs are digital signal pins on an integrated circuit whose behavior (input or output) is controlled by application software. A GPIO is basically a pin that can be configured as an input or an output. If the pin is configured as an output, 1(VDD) or 0 (GND) can be written to this pin. The information on this pin can be read if it is configured as an input respectively. GPIO is a standard interface that allows microcontrollers to communicate with the outside world. It can be used to read values from analog or digital sensors, drive LEDs, drive clocks for I2C communication, and more. In order to inform a connected peripheral that it has been chosen and that a data transfer is about to begin, the APB generates PSEL. The APB PENABLE is used to enable the system to subsequent cycles of an APB data transfer. APB PWRITE is decides read or write operation mode. PWRITE indicates a data write access when asserted logic high ‘1’ and a read data access when deasserted to logic ‘0’.

GPIO consists of several registers such as DIRECTION register, SET register, CLR register, IN and OUT register. For data write access mode PWRITE is set to ’1’. The Direction register configures the direction of I/O port pins. These register are used to determine whether port pins will be utilised as INPUT or OUTPUT. The DIRECTION register is set for output configuration. The PWDATA signal will provide the data for DIR, SET and CLR registers after which comparison takes place and the value is stored into OUT register. The OUT register data is directly access to the pins. Individually each pins can be enable or disable by using SET or CLR registers.

**Pin Discriptions**

I-Input

O-Output

|  |  |  |
| --- | --- | --- |
| **MNEMONIC** | **TYPE** | **NAME AND FUNCTION** |
| PCLK | I | **Clock :**PCLK is the APB interface system clock |
| PSEL | I | **Peripheral Select**: It is used to select a peripheral |
| PRESET | I | **Peripheral Reset:** PRESET input is asserted (‘1’), the APB interface is put into its initial reset state. |
| PENABLE | I | **Peripheral Enable control**: Enable for data transfer |
| PADDR | I | **Peripheral Address**: The bus width is defined by the PADDR parameter and is driven by the APBBridge core. |
| PWRITE | I | **Write select :**PWRITE indicates a data write access when asserted high (‘1’) and a read data access when de-asserted (‘0’) |
| PWDATA | I | **Write Data Bus**: It is driven by the APB4Bridge core during write cycles, indicated when PWRITE is asserted (‘1’). |
| PRDATA | O | **Read data bus :** It is attached peripheral drives this bus during read cycles, indicated when PWRITE is de-asserted (‘0’). |
| PINS[0-7] | O | **GPIO** 8 pins are used. |

**GPIO Register with GPIO signal**

Table 1: GPIO Registers with signals

|  |  |  |  |
| --- | --- | --- | --- |
| **GPIO Signal** | **Control Registers** | **Field** | **Bit Number** |
| Pin[0] | OUT/IN | OUTPUT/INPUT | Bit 0 |
| Pin[1] | OUT/IN | OUTPUT/INPUT | Bit 1 |
| Pin[2] | OUT/IN | OUTPUT/INPUT | Bit 2 |
| Pin[3] | OUT/IN | OUTPUT/INPUT | Bit 3 |
| Pin[4] | OUT/IN | OUTPUT/INPUT | Bit 4 |
| Pin[5] | OUT/IN | OUTPUT/INPUT | Bit 5 |
| Pin[6] | OUT/IN | OUTPUT/INPUT | Bit 6 |
| Pin[7] | OUT/IN | OUTPUT/INPUT | Bit 7 |

**Registers**

The memory-mapped registers for the general-purpose input/output (GPIO)

Table 2: Description of registers

|  |  |  |
| --- | --- | --- |
| **PADDR** | **Function** | **Register Description** |
| 000 | DIR | Direction Register |
| 001 | SET | Set Data Register |
| 010 | CLR | Clear Data Register |
| 011 | OUT | Output Data Register |
| 100 | IN | Input Data Register |
| 101 | - | - |
| 110 | - | - |
| 111 | - | - |

**GPIO Direction Registers (DIR)**

The GPIO direction register (DIR) determines if GPIO pin direction is an input or anoutput.The GPIO direction register (DIR) is shown in below Figure1 and Field Register.

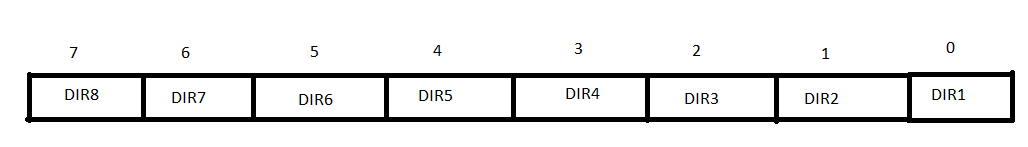


Figure 2: Format for GPIO Direction Registers

**GPIO Direction Register (DIR) Filed Descriptions**

Table 3: GPIO Direction Register (DIR) Filed Descriptions

|  |  |  |  |
| --- | --- | --- | --- |
| **Bit** | **Field** | **Value** | **Description** |
| 0 - 7 | DIR | 0  1 | The Direction register is consists of 8 bits.  It is a GPIO Port Direction Control register and is used to set the direction i.e. either input or output of individual pins.  Direction is set to ‘0’ ->input pins  Direction is set to ‘1’ ->output pins |

**GPIO Output Data Register (OUT)**

The GPIO output data register (OUT) determines the value driven on the corresponding GPIO, if the pin is configured as an output (DIR = 1). The bits in OUT are set or cleared by writing directly to this register.The GPIO Output Data Register register (OUT) is shown in below Figure 3 and Field Register Table 4.

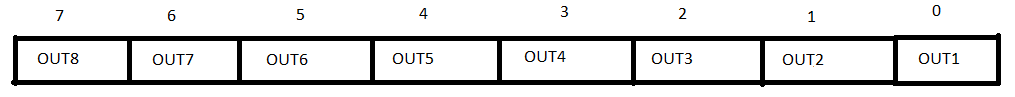


Figure 3: Format for GPIO Output Data Registers

**GPIO Output Data Register (OUT) with Field Descriptions**

Table 4:GPIO Output Data Register Field Descriptions

|  |  |  |  |
| --- | --- | --- | --- |
| **Bits** | **Field** | **Value** | **Description** |
| 0 - 7 | OUT | 0  1 | Output drives state of GPIO pin. The OUTbit is used to store the value drive the output (low =0, high = 1) of pin. when pin is configured asan output (DIR = 1). The OUTbit is ignored when GPIOpin is configured as an input. |

**GPIO Set Data Register (SET)**

The GPIO set data register (SET) controls driving high the corresponding GPIO pin, if the pin is configured as an output (DIR=1), Each individually GPIO Pin can Set high. The GPIO Set Data Register (SET) is shown in below Figure 4 and Field Register Table 5.

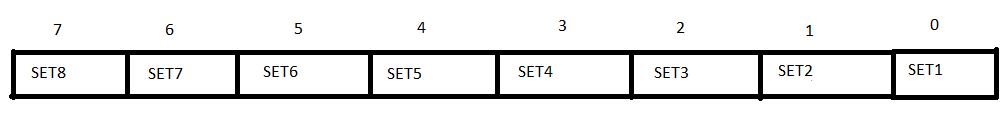


Figure 4: Format for GPIO Set Data Register

**GPIO Set Data Register (SET) with Field Descriptions**

Table 5: GPIO Set Data Register (SET) with Field Descriptions

|  |  |  |  |
| --- | --- | --- | --- |
| Bits | Field | Value | Description |
| 0 - 7 | SET | 1 | The SET Register is consists of 8 bit and individually each bit can be set . It to set a GPIO pin’s output value to High (Logic 1). The  when a bit in the SET register is set to ”1.” for pins highsetting set to ‘0’ has no impact on the pin. |

***GPIO Clear Data Register (CLR)***

The GPIO clear data register (CLR) controls driving low the corresponding GPIO pin, if the pin is configured as an output (DIR= 1). The bits in CLR are cleared by writing directly to this register.The GPIO CLR Data Register (CLR) is shown in below Figure 5.

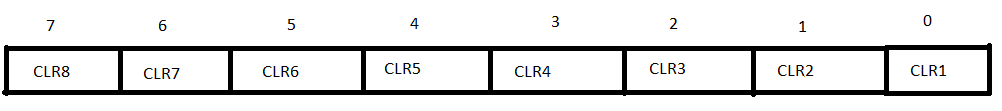


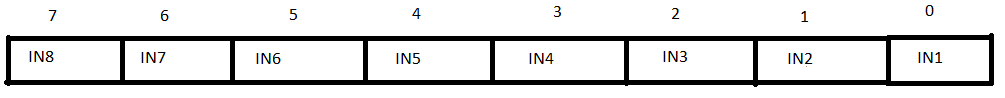
Figure 5: *GPIO Clear Data Register*

**GPIO Clear Data Register (CLR) with Field Descriptions**

|  |  |  |  |
| --- | --- | --- | --- |
| **Bits** | **Field** | **Value** | **Description** |
| 0 - 7 | CLR | 1 | The CLR Register is consists of 8 bit and individually each bit can be clear.  CLR is set to ‘1’ - >clear pin  CLR is set to ‘0’ ->No effect |

**GPIO Input Data Register (IN)**

The current state of the GPIO signals is read using the GPIO input data register, if the pin is configured as an output (DIR= 0).The GPIO Input Data Register (IN) is shown in below Figure 5

Figure 6: GPIO Input Data Register

**GPIO InputData Register (IN) with Field Descriptions**

|  |  |  |  |
| --- | --- | --- | --- |
| **Bits** | **Field** | **Value** | **Description** |
| 0 - 7 | IN | 1  0 | The IN Register is consists of 8 bits.  The IN bit is used to store the value drive the input (low =0, high = 1) of pin. when pin is configured asan input(DIR = 0). The OUT bit is ignored when GPIO pin is configured as an input |

PRESETn input is asserted (‘1’), the APB4 interface is put into its initial reset state.

**Write/Read operation**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **PRESETn** | **PSEL** | **PENABLE** | **PWRITE** | **Function** |
| 0 | 1 | 1 | 0 | Read Access |
| 0 | 1 | 1 | 1 | Write Access |